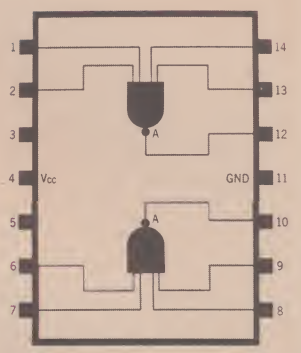
LOW POWER MONOLITHIC TTL ELEMENT

DUAL NAND/NOR GATE DRIVER

SE455J

AUGUST 1966

The SE455J is a semiconductor integrated circuit fabricated within a monolithic substrate by planar and epitaxial techniques. It was designed for maximum speed consistent with extremely low power operation. It is intended for use in applications where high density packaging and the ability to drive high capacitances associated with multilayer printed-circuit boards are important considerations. The SE455J offers two buffer/driver elements in the TO-88, 14 lead flat package. It is compatible with the other elements of the SE400J series under worst-case temperature and power supply variation.

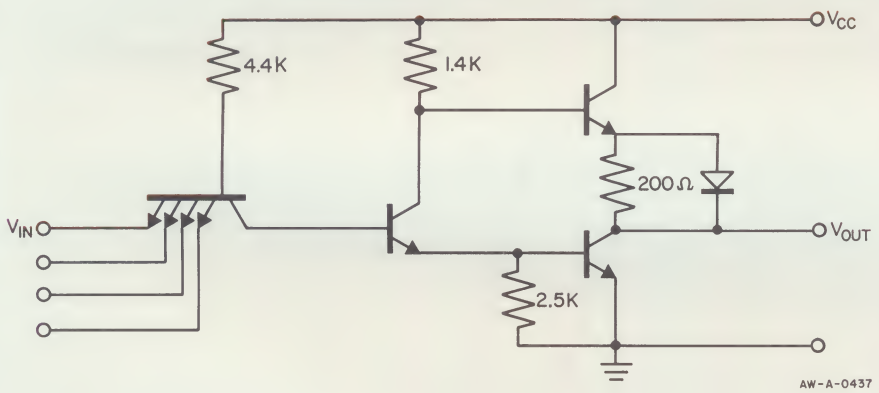


NOTE:
(1) A—Active pull-up

FEATURES

- LOW POWER — 7.0 mW
- HIGH NOISE IMMUNITY — 1.0 volt
- HIGH FAN-OUT — 28
- HIGH SPEED — 28 ns/Gate
- BROAD TEMPERATURE RANGE — −55°C to +125°C

BASIC CIRCUIT SCHEMATIC



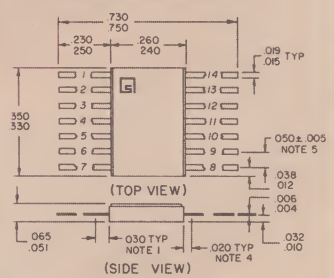
NOTE: ½ of SE455J shown. Component values are typical.

PERFORMANCE GUARANTEE NOTICE

This data sheet is a complete procurement document for the product described. Noise margins, speed, and fan-out are guaranteed from −55°C to +125°C over a broad range of power supply and temperature differentials between driving and driven units. In addition to presenting guarantees immediately applicable by system designers, the needs of component and reliability engineers are met by full details of the quality assurance and reliability programs that stand behind the guarantees. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001.

J-PACKAGE (TO-88)

(MODULAR GLASS-KOVAR)



NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) All dimensions in inches.
(4) Lead spacing dimensions apply to this area only.
(5) Spacing tolerances non-cumulative.

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SE455J

This data sheet has two sections. The first section is a specification table of guaranteed test limits. The second section is a set of general information characteristic curves.

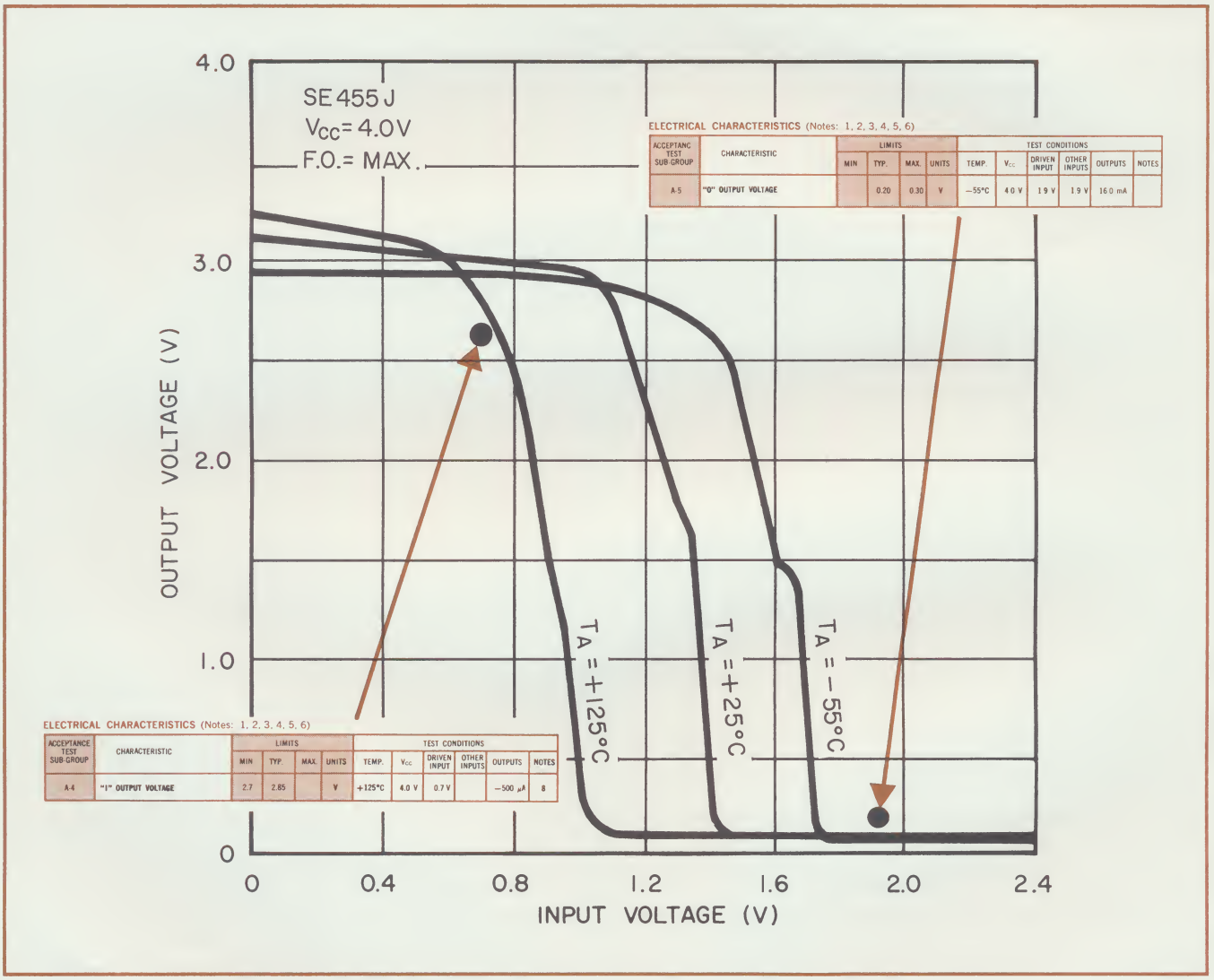
The test limit tables contain a set of parameter test points that are guaranteed by SIGNETICS under the SURE Testing Program. The test points guaranteed cover a broad range of parameters under varying conditions of power supply voltage, loading conditions and environments.

The characteristic curve data are intended to provide the designer with meaningful system design limits over a broader range of operating conditions than do the test limit tables.

The curves are derived from devices selected to assure a high probability that the units used in your system will function well within the design limits you may establish from the characteristic curve data. For the designer who wishes to have characteristic curve points guaranteed, special test points may be established for an additional charge. In most cases, special test point guarantees will be negotiated plus or minus a tolerance from the curve data to take into account test equipment limitations. Please contact your local SIGNETICS' Sales Engineer to discuss special test limit requirements.

Figure 1 depicts graphically the relationship between the test limit tables and the curve data.

FIGURE 1



The data presented in the guaranteed test limit table may be interrelated to determine other meaningful information. For instance, the "I" DCM or noise margin may be calculated for worst case conditions by taking the difference between the minimum "I" output voltage and the minimum "I" input voltage at the worst case temperature and power supply to be encountered in the system. For the "0" DCM or noise margin, calculate the difference between the maximum "0" input voltage and maximum "0" output voltage.

SE455J DUAL NAND/NOR GATE DRIVER

SECTION 1

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNITS	TEMP.	V_{CC}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	**"1" OUTPUT VOLTAGE**	2.7	2.85		V	−55°C	4.0 V	0.9 V		−500 μA	8
A-3		2.7	2.85		V	+25°C	4.0 V	0.9 V		−500 μA	8
A-4		2.7	2.85		V	+125°C	4.0 V	0.7 V		−500 μA	8
C-1		2.3	2.45		V	−55°C	3.6 V	0.9 V		−500 μA	8
C-1		2.3	2.45		V	+25°C	3.6 V	0.9 V		−500 μA	8
C-1		2.3	2.45		V	+125°C	3.6 V	0.7 V		−500 μA	8
C-1		3.1	3.3		V	−55°C	4.4 V	0.9 V		−500 μA	8
C-1		3.1	3.3		V	+25°C	4.4 V	0.9 V		−500 μA	8
C-1		3.1	3.3		V	+125°C	4.4 V	0.7 V		−500 μA	8
A-5	**"0" OUTPUT VOLTAGE**		0.20	0.30	V	−55°C	4.0 V	1.9 V	1.9 V	16.0 mA	
A-3			0.25	0.30	V	+25°C	4.0 V	1.7 V	1.7 V	16.0 mA	
A-4			0.25	0.30	V	+125°C	4.0 V	1.3 V	1.3 V	16.0 mA	
C-1			0.20	0.30	V	−55°C	3.6 V	1.9 V	1.9 V	12.0 mA	
C-1				0.30	V	+125°C	3.6 V	1.3 V	1.3 V	16.0 mA	
C-1			0.20	0.30	V	−55°C	4.4 V	1.9 V	1.9 V	18.0 mA	
C-1			0.25	0.30	V	+125°C	4.4 V	1.3 V	1.3 V	16.0 mA	
C-1	**"0" INPUT CURRENT**			−0.84	mA	−55°C	4.0 V	0.3 V	4.0 V		
A-3		-0.50	−0.65	−0.85	mA	+25°C	4.0 V	0.3 V	4.0 V		
C-1				−0.84	mA	+125°C	4.0 V	0.3 V	4.0 V		
C-1			−0.55	−0.75	mA	+25°C	3.6 V	0.3 V	4.0 V		
C-1			−0.80	−0.96	mA	+25°C	4.4 V	0.3 V	4.0 V		
A-3	**"1" INPUT CURRENT**			10.0	μA	+25°C	4.0 V	3.6 V	0 V		
A-4				20.0	μA	+125°C	4.0 V	3.6 V	0 V		
A-6	**PAIR DELAY**	40	55	85	nsec	+25°C	4.0 V			DC F.O.=22	9
C-2	(Fig. 2)	45	58	95	nsec	+25°C	3.6 V			DC F.O.=22	9
C-2		35	52	85	nsec	+25°C	4.4 V			DC F.O.=22	9
C-2	**OUTPUT FALL TIME**		35	50	nsec	+25°C	4.0 V			AC F.O=8	10
A-6	(Fig. 3)		60	75	nsec	−55°C	3.6 V			AC F.O.=8	10
C-2	**INPUT CAPACITANCE**			3.0	pf	+25°C	4.0 V	2.0 V			7
	POWER CONSUMPTION (Per Gate)										
A-4	OUTPUT "0"		12.5	15.6	mW	+125°C	4.0 V				
C-1	OUTPUT "0"		10.0	13.3	mW	+125°C	3.6 V				
C-1	OUTPUT "0"		15.5	19.3	mW	+125°C	4.4 V				
A-2	OUTPUT "1"		3.0	4.0	mW	+25°C	4.0 V	0 V			
C-1	OUTPUT "1"		2.5	3.3	mW	+25°C	3.6 V	0 V			
C-1	OUTPUT "1"		4.0	5.3	mW	+25°C	4.4 V	0 V			
A-2	**INPUT VOLTAGE RATING**	6.0			V	+25°C	4.0 V	50μ A			
A-2	**OUTPUT SHORT CIRCUIT CURRENT**	−20		−80	mA	+25°C	4.0 V	0 V		0 V	

NOTES:

(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

(2) All measurements are taken with Pin 11 tied to zero volts.

(3) Positive current flow is defined as into the terminal referenced.

(4) Positive NAND Logic definition: "UP" Level="1", "DOWN" Level="0".

(5) Precautionary measures should be taken to insure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.

(6) Measurements apply to each gate element independently.

(7) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1 MHz, V_{AC} = 25 mV_{RMS}. All pins not specifically referenced are tied to guard for capacitance tests.

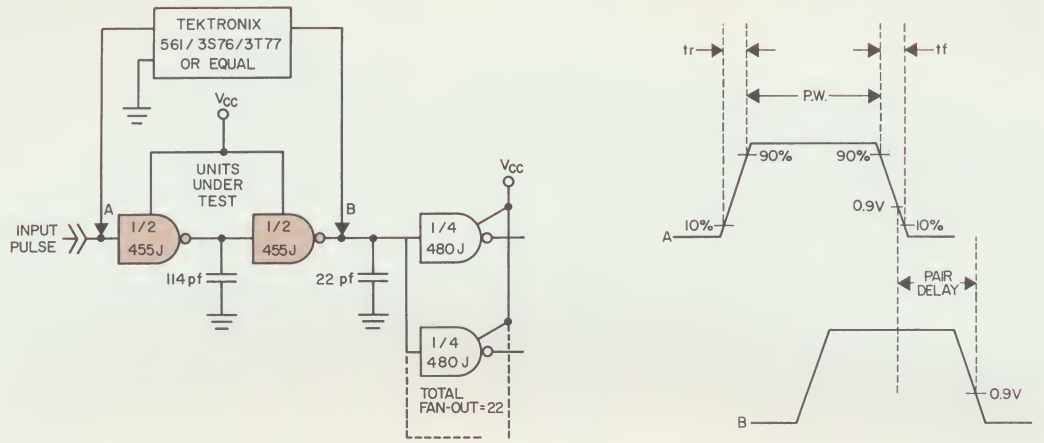
(8) Output leakage current is supplied through a resistor to ground.

(9) D.C. Fan-out is defined in terms of a SIGNETICS Standard Unit Load, which is an SE480J gate input or an equivalent impedance.

(10) One AC Fan-out is defined as equivalent to one clock pulse input of an SE424J or a 50 pf capacitance load.

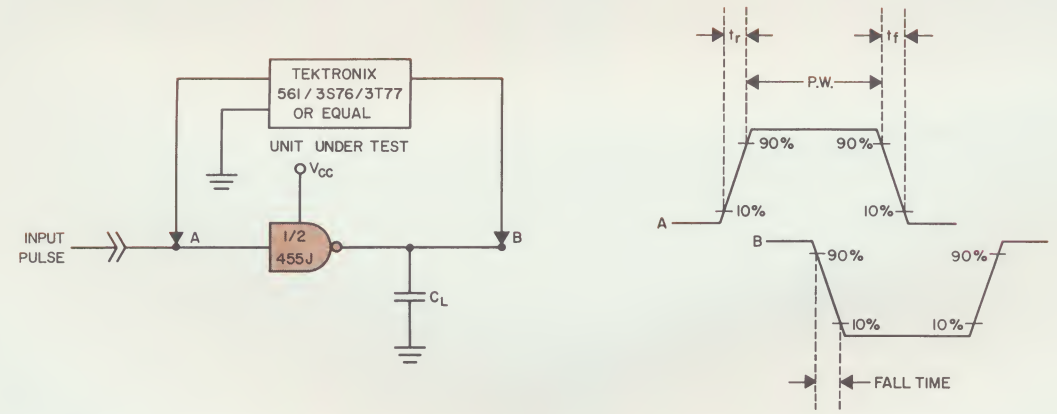
SECTION 1

FIGURE 2 — PAIR DELAY



NOTES: (1) Capacitance values shown include probe and test fixture capacitance.
(2) Input Pulse Characteristics: Amplitude=+2.7 V; f=1.0 MHz; PW=350 ns; t_r=t_f=10 ns.

FIGURE 3 — FALL TIME



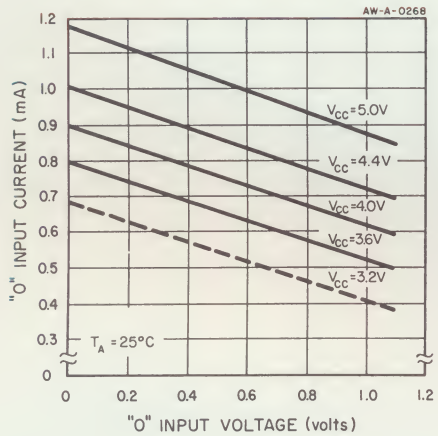
NOTES: (1) C_L includes test fixture and probe capacitance. C_L=462 pf for fan-out of 8 and 77 pf for fan-out of 1.
(2) Input Pulse Characteristics: Amplitude=+2.7 V; f=1.0 MHz; PW=200 ns; t_r=t_f=10 ns.

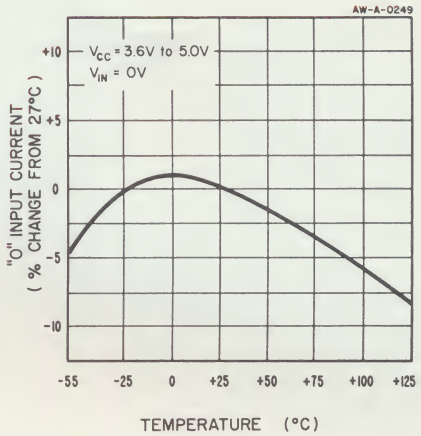
ABSOLUTE MAXIMUM RATINGS:

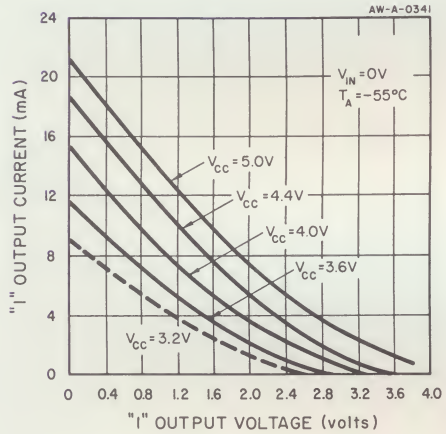
INPUT VOLTAGE	6.0V	OPERATING TEMPERATURE	-55°C to +125°C
V_{cc}	6.0V	STORAGE TEMPERATURE	-65°C to +150°C
INPUT CURRENT	±10mA	Θ_{J-A} (R_{TH} Junction to Still Air)	0.3°C/mW
OUTPUT CURRENT	±100mA	JUNCTION TEMPERATURE	150°C MAX.

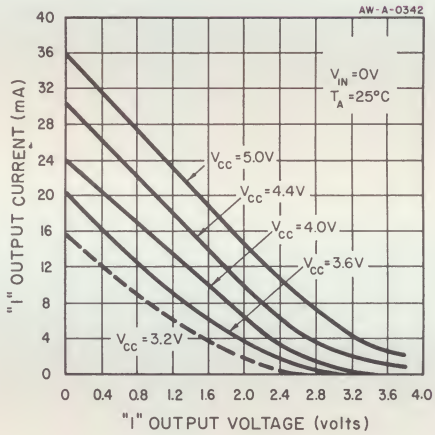
Maximum ratings are limiting values above which serviceability may be impaired.

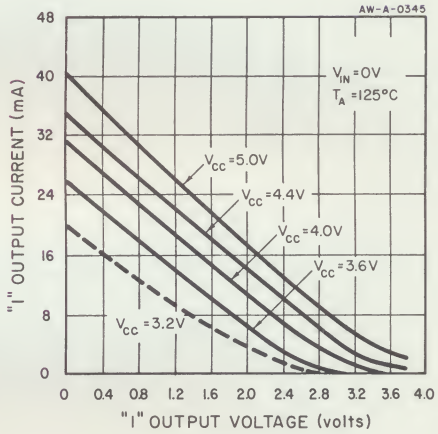
SECTION 2 — SYSTEM DESIGN LIMIT CURVES

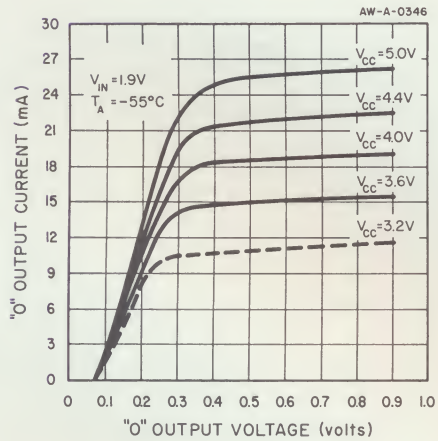


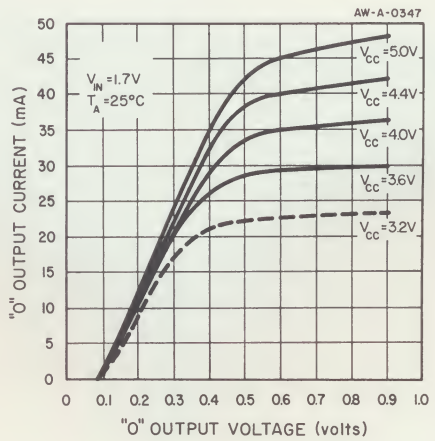


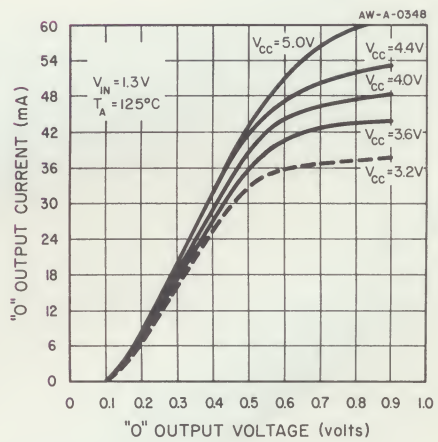




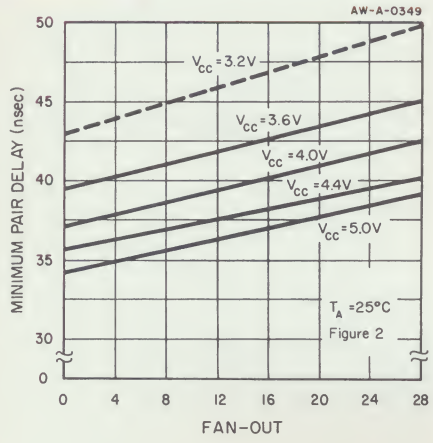


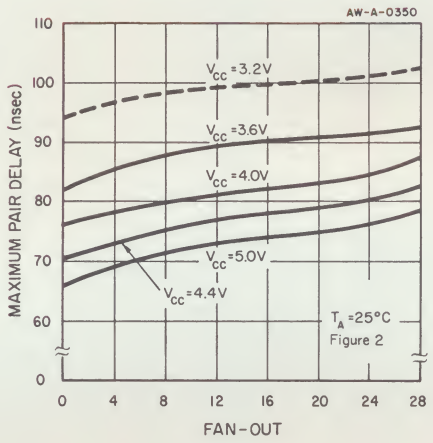


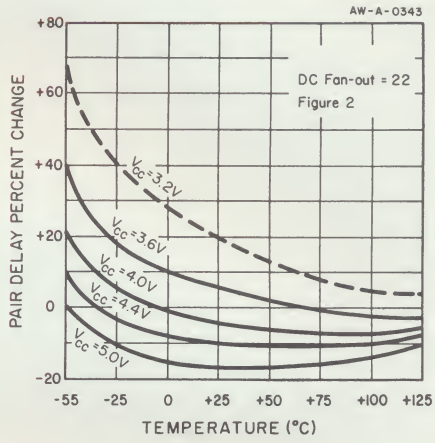


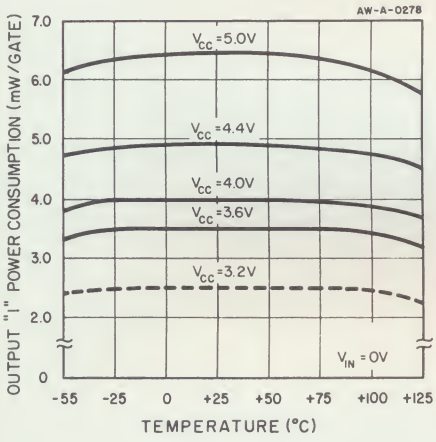


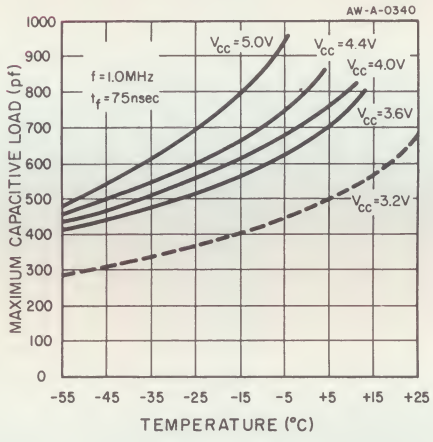
SECTION 2 — SYSTEM DESIGN LIMIT CURVES



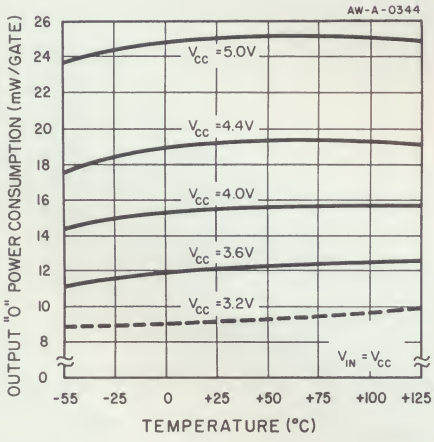


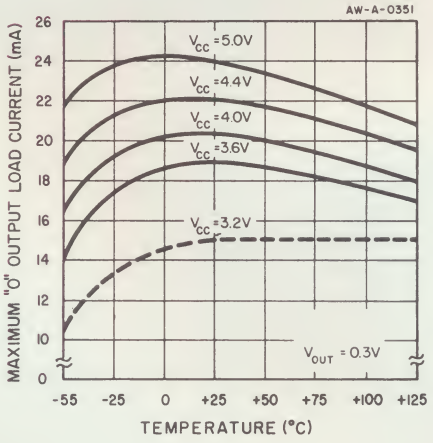






"Maximum Capacitive Load vs. T_A" depicts AC fan-out capability for the SE455J in terms of capacitance driven when the output fall time is restricted to 75 ns maximum. One AC fan-out is defined as equivalent to one clock input of an SE424J (50 pf maximum). The SE424J clock input pulse fall time should not exceed 75 ns. Since AC fan-out is limited to 8 under worst case conditions, the curve only extends to 25°C.





"Maximum "0" Output Load Current vs. T_A" depicts DC fan-out in terms of output current sinking capability. DC fan-out may be derived by determining the output current capability under the appropriate conditions from the curve and dividing by the appropriate Input "0" Current for the driven element.

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